Design and Verification of Synchronous FIFO using SystemVerilog

The Synchronous FIFO module operates on a synchronized clock signal, facilitating orderly data handling. Write operations involve inserting data into the FIFO while read operations retrieve data in the order it was written. Pointer management mechanisms are employed to track the current read and write positions within the FIFO, ensuring seamless data retrieval and insertion. SystemVerilog is utilized for testbench development, enabling thorough verification of the FIFO module's functionality.

# Expected outcomes

* **Design of Synchronous FIFO Module**: A fully operational Synchronous FIFO module meeting design specifications and requirements. The FIFO should facilitate synchronized data transfer, ensuring that data is read out in the same order it was written, without loss or corruption.
* **Complete SystemVerilog Testbench for Verification**: A comprehensive testbench developed in SystemVerilog to thoroughly verify the functionality of the FIFO module. The testbench should cover various test scenarios, including edge cases and corner cases, to validate the FIFO's behavior under different conditions.